REMARKS

The foregoing amendments and the following remarks are deemed fully responsive to the pending office action of June 20, 2005. Claim 1 is amended to limit the first identifier to be within the memory access request as shown in FIG. 2 of the drawings and described in paragraph [0030] of the specification. Claim 7 is amended to depend from claim 5 and not claim 6. Claim 14 is amended to limit initiation of speculative memory access requests to within a CPU as shown in FIG. 1 and described in paragraphs [0028-0029]. Claim 16 is amended for clarity. Claim 20 is added to depend from claim 16 and include limitations removed from claim 16. No new matter is added. Claims 1-20 are pending, of which claims 1, 14 and 16 are independent.

Claim Objections

Claim 7 stands objected to under 37 CRF § 1.75(c), as being of improper dependent form. Claim 7 is therefore amended to depend from claim 5. Reconsideration of claim 7 is respectfully requested.

Claim Rejections – 35 U.S.C. § 112

Claims 1-15 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter. Respectfully, we disagree.

Claim 1 recites a method for processing a memory access request (see FIG. 2) within processing architecture. As shown in FIG. 1, the processing architecture includes a CPU 12, an instruction cache 18, a system bus 16 and a main memory 14. The steps of the method (see FIG. 3) thus apply to each component of the processing architecture. For example, instruction cache 18 determines whether the memory access request is speculative or not based upon a first identifier of the memory access request, assesses interconnect resource condition in the event that the memory access request is speculative and either processes the memory access request, or not, as a function of the condition. Similarly, a memory controller within main memory 14 determines whether the memory access request is speculative or not based upon a first

identifier, assesses target resource condition in the event that the memory access request is speculative and either processes the memory access request, or not, as a function of the condition. However, if instruction cache 18 does not process the memory access request based upon interconnect resource conditions, main memory 14 does not even receive the memory access request, and therefore has nothing to process. Thus, it is not always necessary to determine target resource conditions.

It should be appreciated that the processing architecture is distributed, in that components of the architecture may be connected by one or more buses (e.g., system bus 16), and therefore each of these components may determine, assess and selectively process speculative memory access requests. As taught by paragraph [0008] of the specification, "a bus controller, switch or other logic device coupled with the bus elects to either carry out speculative transactions, or not, depending upon traffic or saturation conditions on the bus or within target memory." Further, paragraph [0011] teaches that logic components linked to the processing architecture – e.g., switches or bus controllers, may independently decide to act, or not, on speculative transactions.

Clearly, depending upon where the congestion occurs, one or both of conditions may be assessed.

Reconsideration of claims 1-15 is respectfully requested.

Claim Rejections – 35 U.S.C. § 102

Claims 1-19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,654,860 issued to Strongin et al. (hereinafter "Strongin"). Respectfully, Applicant disagrees.

To anticipate a claim, Strongin must teach every element of the claim and "the identical invention must be shown in as complete detail as contained in the ... claim." *MPEP 2131* citing *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987) and *Richardson v. Suzuki Motor Co.*, 868 F2.d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989). Strongin does not teach every element of claims 1-19.

As background, the '971 Application teaches of a method for processing a memory access request within a processing architecture. The memory access request is generated, for example, within a central processing unit (CPU) of the processing

architecture. Each component (e.g., bus controller, switch or other logic device) of the processing architecture may selectively process the memory access request based upon if the memory access request is speculative and traffic conditions on the bus or congestion of target memory. See at least paragraph [0008] of the specification.

On the other hand, Strongin discloses a memory controller that generates speculative and non-speculative memory access requests. See Strongin abstract. The method and apparatus of Strongin operates only within the memory controller which is located in a Northbridge. See at least Strongin FIG. 4A. Operation of Strongin is therefore constrained to within the Northbridge; Strongin does not selectively process memory access requests over a bus external to the Northbridge, nor assess traffic on a bus to determine whether to process a speculative memory access request, or not.

Amended claim 1 recites a method for processing a memory access request within processing architecture, including the steps of:

a) determining whether the memory access request is speculative or not based upon a first identifier of the memory access request;
b) assessing one or both of interconnect and target resource conditions in the event that the memory access request is speculative; and
c) either processing the memory access request, or not, as a function of the conditions.

The Examiner asserts that Strongin assesses traffic conditions of PCI bus 118 in order to determine its availability. Applicants respectfully disagree. In Strongin, the memory controller 400 generates speculative memory access requests within Northbridge 104. See Strongin col. 22, lines 47-55. It would make no sense for Strongin to assess PCI bus 118, which is external to Northbridge 104, when determining whether to process these speculative memory access requests since PCI bus 118 does not influence further processing of these requests. Nowhere does Strongin suggest that PCI bus 118 influences processing of speculative memory requests. Therefore, Strongin cannot anticipate, at least, step b) of claim 1. Further, Strongin does not disclose or suggest that the memory access request received at the Northbridge via the PCI bus 118 (or any other bus) includes an indicator that it is speculative. Specifically, Strongin generates the speculative memory access requests with the memory controller, and shows tags 502 within reorder buffer 600, and not

within a memory access request received by the memory controller. See Strongin FIG. 6A. Strongin cannot, therefore, anticipate step a) of claim 1.

Reconsideration of claim 1 is respectfully requested.

Claims 2-13 depend from claim 1 and benefit from like argument. However, these claims have additional features that patentably distinguish over Strongin. For example, claim 2 recites decoding the first identifier as a first bit field within the memory access request. Strongin discloses a tag 502 within re-order buffer 600 (see Strongin FIG. 6A), but does not disclose or suggest a bit field within memory access requests as required by claim 2.

Claim 3 recites encoding the first bit field within the memory access request to define a speculative ID of the memory access request. Again, Strongin does not disclose a memory access request that includes a speculative ID.

Claim 4 recites the memory access request comprises one of an instruction, a message and an operational request. Strongin does not disclose or suggest a memory access request with an instruction, a message and an operational request. In FIG. 6A and 6B, Strongin shows a re-order buffer 600 and does not show a memory access request with an instruction, a message and an operation request.

Claim 5 recites determining a priority of the memory access request based upon a second identifier, in the event that the memory access request is speculative, and wherein the step of processing the memory access request comprises processing the memory access request, or not, based upon the conditions and the priority.

Claim 6 recites decoding the second identifier as a second bit field within the memory access request. Claim 7 recites encoding the second bit field within the memory access request to define a priority of the memory access request. Strongin shows an urgency field within tag 502 of reorder buffer 600, but does not show a bit field within a memory request. Claim 9 recites utilizing one of a CPU, chipset and memory controller to determine whether the memory access request is speculative. Strongin operates only within memory controller 400 of Northbridge 104, and does not disclose or suggest utilizing one of a CPU, chipset and memory controller to determine whether the memory access request is speculative.

Claim 10 recites at least one of the CPU, chipset and memory controller independently controls the step of processing the memory access request based on the

conditions. Claim 11 recites assessing one or more of memory utilization, memory congestion, buffer space utilization, and bus congestion. Claim 12 recites assessing one or more of bus utilization, bus congestion, crossbar utilization, cross bar congestion, and point to point link utilization. As argued above, Strongin does not assess one or more of bus utilization, bus congestion, crossbar utilization, cross bar congestion, and point to point link utilization.

Claim 13 recites notifying one or more logic devices when the memory access request is not processed. Contrary to the Examiner's assertion, Strongin does not disclose notifying one or more logic devices when the memory access request is not processed. As argued above, Strongin operates only within the Northbridge device.

Reconsideration and allowance of claims 1-13 are requested.

Amended claim 14 recites CPU architecture that initiates both speculative and non-speculative memory access requests within a CPU, an improvement including decode logic for determining whether the memory access requests are speculative, and assessment logic for determining one or both of interconnect and target resource conditions, the CPU architecture processing speculative memory access requests, or not, as a function of the conditions. Strongin does not disclose initiating both speculative and non-speculative memory access requests with an CPU. As argued above, Strongin discloses generating speculative memory access requests only within the Northbridge, and cannot, therefore, anticipate claim 14 for at least this reason.

Claim 15 depends from claim 14 and benefits from like argument. Reconsideration of both claims 14, 15 are requested.

Amended claim 16 recites a system for processing speculative memory access requests within a processing architecture, comprising:

a) one or more memory access requests having a bit field defining the memory access requests as speculative or non-speculative;
b) decode logic for decoding the bit field to determine whether one or more memory access requests are speculative; and
c) processing logic for processing speculative memory access requests, or not, based on interconnect conditions.

As argued above, Strongin does not disclose a memory access request having a bit field defining the memory access requests as speculative or non-speculative as

required in element a) and therefore cannot anticipate elements a) and b). Further, Strongin does not disclose or suggest processing logic for processing speculative memory access requests, or not, based on interconnect conditions as required in element c). Strongin cannot therefore anticipate claim 16.

Reconsideration of claim 16 is respectfully requested.

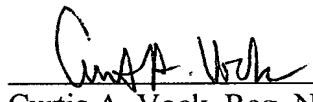
Claims 17-20 depend from claim 16 and benefit from like argument. For at least this reason, Strongin cannot anticipate claims 17-20.

Reconsideration of claims 17-20 is respectfully requested.

For the reasons discussed above, Applicant believes that amended claims 1-20 are not anticipated by Strongin. Reconsideration and allowance of all claims are requested.

Applicants believe no fees are due in connection with this Amendment and Response; however, if any fee is deemed necessary, the Commissioner is authorized to charge such fee to Deposit Account No. 08-2025.

Respectfully submitted,

By: 

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